Nanometer DFM – The tip of the ice

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1 Abstract

Design for manufacturing has become one of the key factors of nanometer designs for the past decade and it is facing increasing challenges from the manufacturing limitations. These manufacturing and process challenges include the printability issues due to deep sub-wavelength lithography, the topography variations due to chemical-mechanical polishing (CMP), the random defects due to missing and extra material, the via void, and more. Another necessity is corrections of optical process effects (optical proximity correction (OPC) and phase-shifting masks (PSM)) which create entire layout design and verification methodologies. Classic DFM design (Design for Manufacturing) consists of an analysis of yield and a set of constraints. These constraints are imposed as both guidelines and by creating an MRC (manufacturing rule check) deck. The majority of the yield loss is strongly layout-dependent thus manufacturability aware layout optimization is playing a key role in the overall yield improvement. Reticle enhancement technologies (RET) like optical proximity correction (OPC) and phase shift masking (PSM) have significantly increased the cost and complexity of nanometer photomasks. The photomask layout is no longer an exact replica of the design layout. As a result, reliably verifying RET synthesis accuracy, structural integrity, and conformance to mask fabrication rules are crucial for the manufacture of nanometer regime VLSI designs. New EDA systems consists of efficient wafer-patterning simulators that is able to solve the process physical equations for optical imaging, resist development and hence can achieve high degree accuracy required by mask verification tasks. These tools are able to efficiently evaluate mask performance by simulating edge displacement errors between wafer image and the intended layout. Our discussion addresses the necessary changes in the design-to-manufacturing flow, including infrastructure development in the mask and process communities as well as opportunities for research and development in IC physical layout, routing and verification stage. Although there are other manufacturability aware efforts in earlier design stages such as logic synthesis and placement, the physical design stage coverage is often believed to be one of the most effective design phases to address the manufacturability issues. Creating physical design methodologies to cover manufacturing issues (Topography variation due to CMP, random defects, lithography, and redundant vias) are tightly coupled with interconnection network which is mainly determined by routing and layout connectivity. Major academic and industrial efforts are invested for the past decade to provide efficient nanometer *manufacturability* solutions.

2 Introduction

In the nanometer era, which the wavelength of lithographic printing is greater than the design half pitch (sub-wavelength design), a new paradigm is required for a manufacturing-aware design – one that affects the design flow fundamentally and also adds much complexity to the mask data preparation (MDP) process. As designs step into 90 nm, 65 nm and below they can be characterized by a significant reduction of lithographic contrast, K1. This creates a whole new world of

implications. One of the major issues is that the lithographic process is not synchronized with the original physical design pattern. Even at perfect imaging focus and exposure, results in fabricated IC pattern elements that are no longer a faithful replica of the original physical design. In addition, manufacturing margin is much reduced. This phenomenon has a direct impact on the cost due to the fact that new methods have to be invented to recover some of the imaging fidelity, improving the range of focus and exposure that produce accurate thin film patterns on silicon.

3 The sub-wavelength gap

These goals are partially achieved by modifying MDP to include resolution enhancement technologies (RET). These technologies modify the mask shapes from those of the physical design such that the fabricated shapes are much closer to the physical design, while the shapes on the mask themselves are an input to the highly nonlinear transformation caused by the low K1 lithographic systems. Successful RET strategies also solve the second issue, that of manufacturing tolerance. When this strategy is well implemented, the result is more exact fabrication that is more correlated with the design intent, and with much improved yield in the presence of variations in manufacturing parameters.
In the high K1 area, mask shapes are equal to actual silicon shapes and also print with good manufacturing tolerance. Figure 1 shows the sub-wavelength gap.

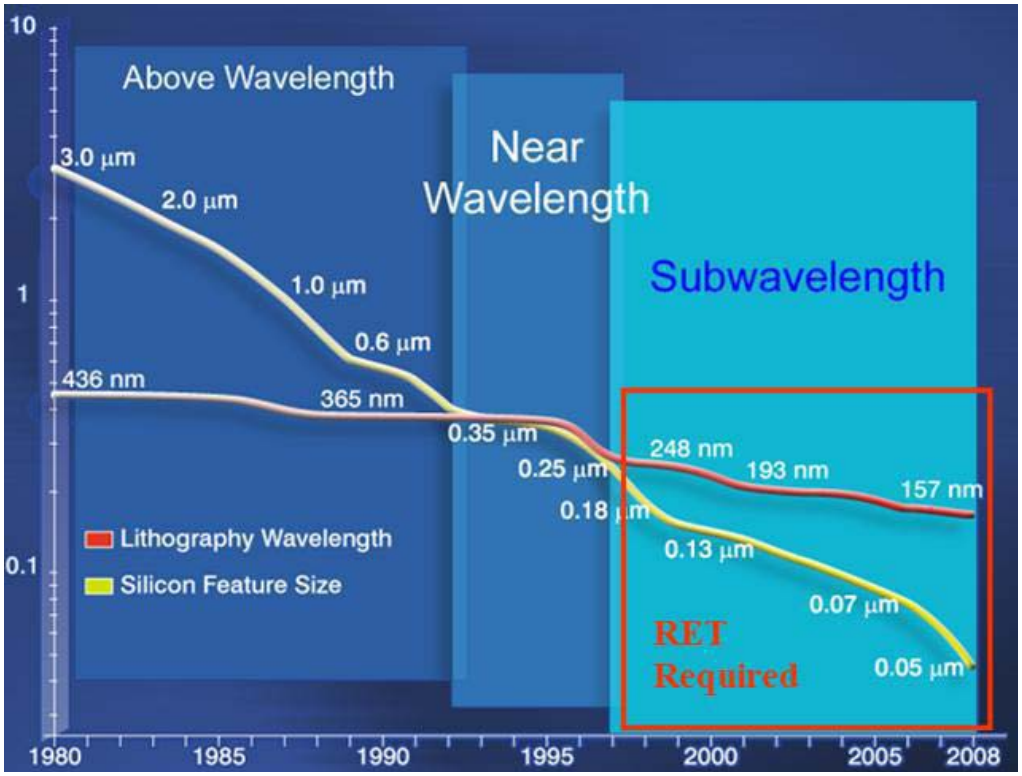


Figure #1 - The Sub-Wavelength Gap

4 Key Manufacturability Issues

In this section, we provide an overview of the major manufacturing issues for 90*nm* technology and below. We will also analyze the causes and effects of these phenomenons:

1. Printability issues due to sub-wavelength lithography system - The printability issue arises between neighboring wires and vias due to sub-wavelength effects and process variations. Tremendous efforts are constantly done in the Resolution Enhancement Techniques (RET) in order to provide solutions for printability. However, if the initial design is not providing a full coverage for lithography, even aggressive RET may not be able to solve the printability problem. The physical design phase and mainly routing and interconnections should be constructed using litho-aware technology in order to avoid late printability issues. A litho-aware connectivity and routing is more general than the restrictive design rules (RDR), which has mostly been adopted so far for the poly-layer design type.

2. Random defects due to missing/extra material - Smaller feature size makes nanometer VLSI designs more vulnerable to *random defects*, which can be further divided into open or short defects. Both defects are one of the back-end-offline (BEOL) defects and cause electrical open or short between interconnects. While it is generally believed that the yield loss due to systematic sources is greater than that due to random defects during the technology and process ramp-up stage, the systematic yield loss can be largely eliminated when the process becomes mature and systematic variations are extracted or compensated.
On the other hand, the random defects which are inherent due to manufacturing limitations will still be there even for mature fabrication process. Thus, its relative importance will indeed be bigger for mature process with systematic variations designed in.

3. Optical Proximity Correction (OPC) - Optical Proximity Correction is the process of modifying the polygons that are drawn by the designers to compensate for the non-ideal properties of the lithography process. Given the shapes desired on the wafer, the mask is modified to improve the reproduction of the critical geometry. This is done by dividing polygon edges into small segments and moving the segments around, and by adding additional small polygons to strategic locations in the layout. The addition of OPC features to the mask layout allows for tighter design rules and significantly improves process reliability and yield. OPC is became a must in early nanometer processes and is a significant component within any DFM considerations. (Figure #2)

4. Topography variations due to chemical-mechanical polishing (CMP) - *Topography (thickness) variation* due to dishing and erosion after CMP is shown to be systematically determined by wire density distribution. Even after CMP, intra-chip topography variation can still be on the order of 20-40%. Such topography variation leads to not only significant performance degradation due to increased wire resistance and capacitances, but also acute manufacturing issues like etching and printability due to defocus. The main reason for CMP problems is wire density distribution. Higher wire density usually leads to copper thickness reduction due to

erosion after CMP, making resistance worse. Also, the reduced copper thickness after CMP can worsen the scattering effect, further increasing resistance. (Figure #5)

5. Phase Shift Mask (PSM) - A “phase conflict” is a difficult problem in phase shift mask (PSM) technology. This conflict arises from unintentionally joining two regions that transmit light with opposite phases. Destructive interference of these two light creates artificial features on wafer. Such conflict is practically unavoidable in any PSM designed for printing real patterns of integrated circuits. How to eliminate these artificial features is a major issue in PSM technology. Researchers have developed several approaches to handle this issue. Some of them have been implemented in real production while others still in experimental stage. Among those approaches used in manufacturing, Complementary Phase Shift Mask (CPSM) technology has demonstrated the power to improve exposure process window significantly, and has been chosen by major semiconductor companies for their deep sub-wavelength lithography process. However, the CPSM technology has its own serious problems. Therefore other alternative PSM technologies are constantly under massive research by the industry and academics. With the advancements of nanometer processes this issue is becoming a major obstacle for manufacturability. (Figure #3)

6. Manufacturability causes such as via failure and antenna effect - A via may fail due to various reasons such as random defects, electromigration, cut misalignment, and/or thermal stress induced voiding effects. Redundant via (or double via) can be inserted as a fault-tolerant replacement for the failing one. Redundant via is known to be highly effective, leading to 10-100x lower failure rate. During fabrication process, charges from plasma etching can be accumulated in long floating wires. Such charges may create high current to the thin-oxide gate (Fowler-Nordheim tunneling current), and cause permanent damages to the gate. It is known as the *antenna effect*. There are three kinds of solutions to prevent the antenna effect: protection diode embedding, diode insertion after placement and routing, and jumper insertion. While the first two solutions need extra area for diode, the jumper insertion incurs overhead in routing system due to additional vias. (Figure #4)

These challenges must be addressed within every nanometer process on order to optimize the yield. The physical design phase ought to include Manufacturability-Aware technology in order to construct interconnections and routing that are DFM compliant.

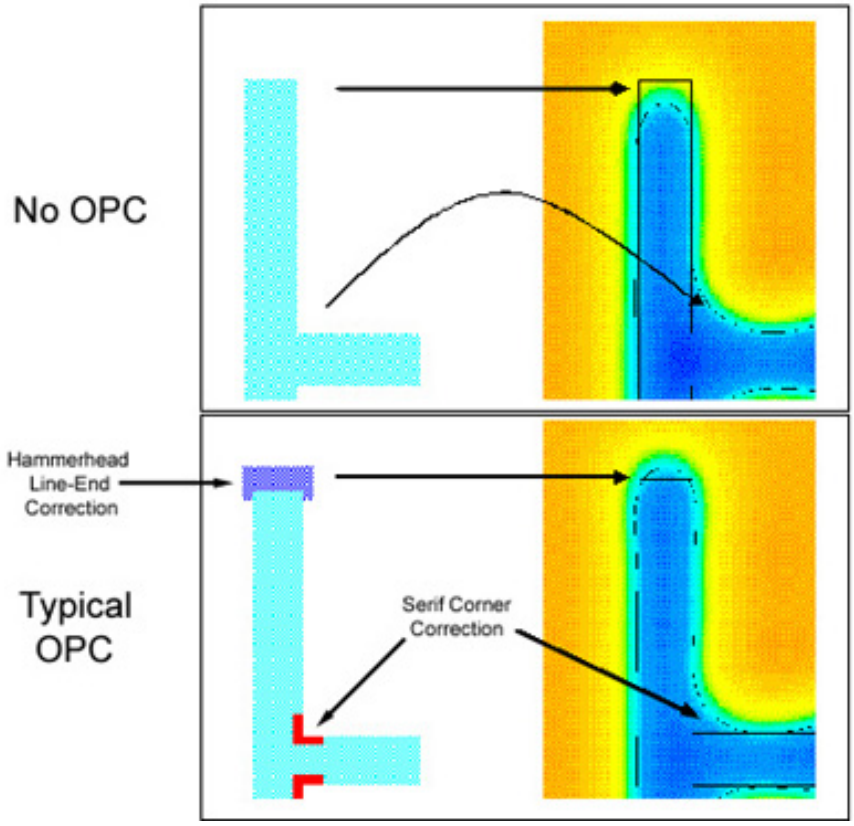
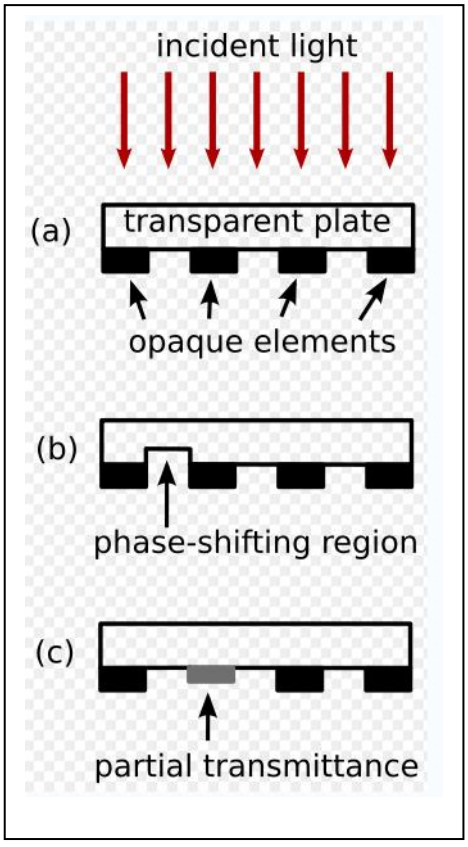


Figure #2 – Optical Proximity Correction
Image Source: Synopsys

Figure #3 – A schematic illustration of various types of masks: (a) a conventional (binary) mask; (b) an alternating phase-shift mask; (c) an attenuated phase-shift mask.

Image Source: Wikipedia



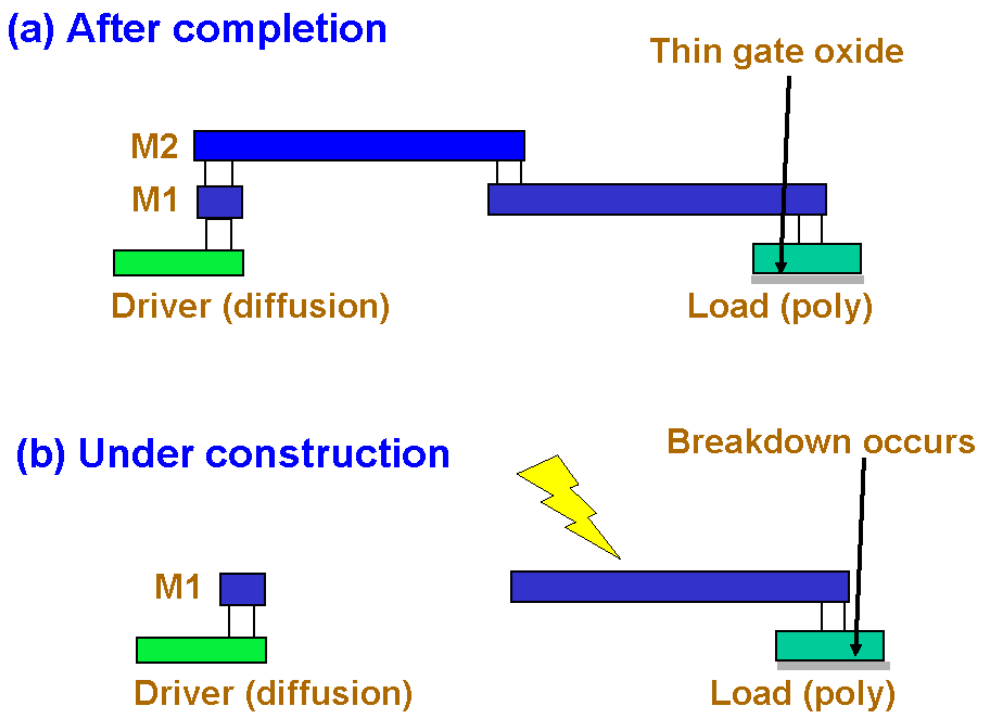


Figure #4 – The cause of antenna effect.

(M1 and M2 are the first two metal interconnect layers.)

Image Source: Wikipedia

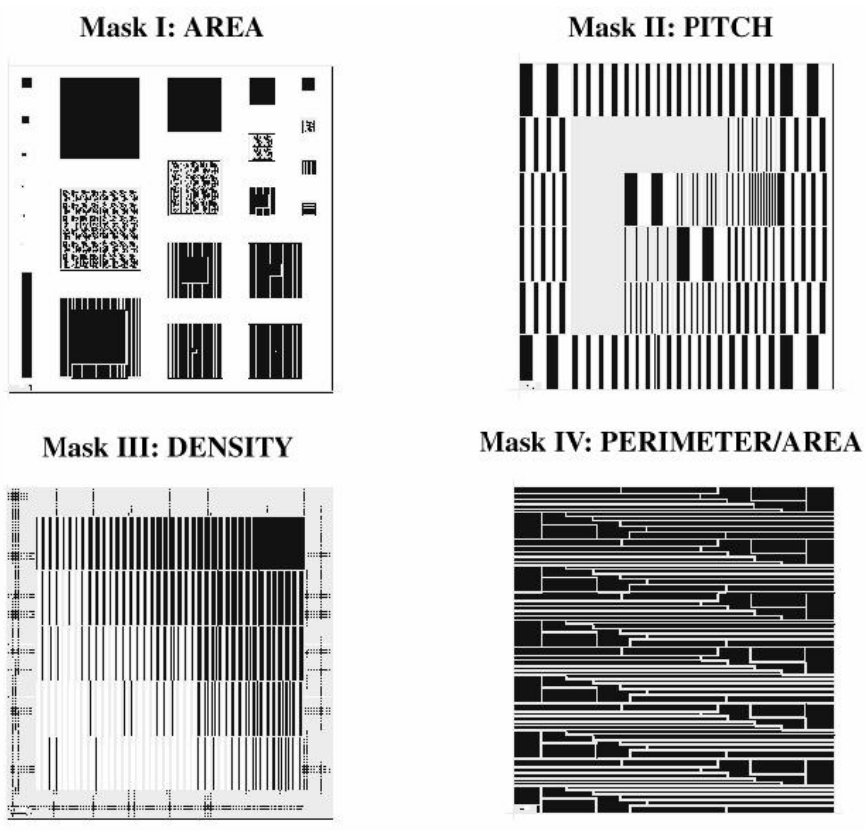


Figure #5 – Oxide CMP Characterization Mask Set.

Image Source: Berkeley

5 Manufacturability-Aware Physical Design Aspects

5.1 RET implementation

Reticle enhancement technologies for nanometer manufacturing has dramatically complicated the mask data and increased the cost of advanced photomasks. The increase in pattern complexity due to optical proximity correction (OPC), the tight requirements for Critical Dimension (CD) control, and the difficulties in defect inspection and repair all contribute to the manufacturing cost increase. For phase shift masks (PSM), the problems are compounded by additional requirements such as controlling the etching of multiple materials, alignment of multiple layers, and inspecting small defect with weak signals. In addition to the added complexities in mask making, the growing array of Reticle Enhancement Technologies (RET) also put more constraints on the physical layout design and verification as physical layouts must be RET compliant and conform to the mask fabrication rules. This more complex flow creates RET-imposed distortions of the design shapes based on models of the mask writing and lithographic processes. By basing RET corrections on calibrated models of mask and fabrication, one can substantially compensate for the insufficient transfer function and manufacturing margins of the low contrast lithographic system. Unfortunately, this flow does not guarantee adequately accurate replication of the design shapes to guarantee success. The fabricated thin film pattern distortions may create shorts and opens (yield issues), electromigration hot spots (reliability issues), or changes in electrical parasitics that fatally impact electrical functionality. Consequently, as is the case with electrical function-based design automation, verification of the result is essential to productizing the design. In this flow, verification is either accomplished by a full chip simulation tool or by measuring the actual silicon result. This methodology requires advanced EDA tools in order to overcome yield and signal integrity issues.

5.2 Physical Design interconnect & Routing implementation

The IC's Physical Design phase's interconnection and routing can be categorized into *rule-based* approach and *model-based* approach. The layout's interconnections and routing is a major challenge in order to achieve manufacturability compliancy. We will present some of the advantages and disadvantages of interconnect and routing approaches in terms of complexity and efficiency.

Rule-based approach extends the conventional *design rules*, i.e., a set of rules which must be observed by the designers and/or automatic tools, by introducing a new set of manufacturability-aware rules. These new manufacturability aware rules can be *required/hard* rules, or *recommended/soft* rules. Since existing routing systems have been based on design rules for decades, rule-based approach is friendly to the conventional design flow, which makes it seemingly easy to implement and apply. However, there can be several problems with rule-based approach.

1. The number of such manufacturability aware rules is increasing exponentially with each new technology process. For example, while the number of rules is only a few hundred at 65*nm* process, it reaches several thousands in 45 and 32nm processes. The same design rule may work differently in deep nanometer processes depending on the design context.
2. The complexity of checking such rules becomes more computationally expensive, as the rules are increasingly context-sensitive. For example, the minimum spacing between wires may depend on the wire lengths, the

neighborhood wires, as shown in an example in Fig. 1. Therefore, simply checking rules by itself needs considerable amount of computing resource.

3. The rules are binary in nature, i.e., either following the rule or violating the rule, thus the rule-based approach does not provide smooth tradeoff.
4. The rules themselves may be too restrictive and pessimistic to sacrifice performance. In some cases, it may be infeasible to achieve the performance goals due to over guard-band from the rules. Furthermore, the rules may not be accurate enough to model very complicated manufacturing processes, in particular for the future deeper sub-wavelength lithography systems. Due to these limitations of the rule-based approach, there have been significant ongoing efforts in the model-based approach at both academia and industry, expecting that models will capture manufacturing effects more accurately at affordable computational overhead coupled with a small number of simple design rules. For example, this may include lithography system modeling where the light will pass through the mask and react with the chemicals on the surface of the wafer, resulting in printed structures. The challenge with model-based approach is how to abstract a set of reasonably accurate yet high fidelity models at various abstraction levels to guide physical layout optimizations. A typical manufacturing system involves nonlinear optical, chemical, electrical, and mechanical processes which could be extremely complicated to model accurately and mathematically. On the other hand, the models have to be compact and efficient to be embedded in the already time-consuming VLSI routing system. Therefore, the key technical bottleneck for model-based manufacturability aware routing is to develop simple/compact yet effective/high-fidelity models, and apply them to existing routing flow in a seamless manner.

5.3 RET Driven Design

One-Pass successful design is the way that the industry is aiming towards. In this strategy, the building blocks of the design are optimized for sub-wavelength fabrication before the large-scale, full-chip integration of these blocks occurs. Figure 4 show one way in which the design paradigm can be fundamentally changed to guarantee fabrication robustness. On the left side of Figure 4 is an optimization loop in which circuit blocks are put through a virtual manufacturing flow to certify them for manufacturability. These blocks are usually pre-designated (design IP) and can come from many sources. These can be internal to the company creating the design as well as external, e.g. schematics or physical blocks for industry standard busses, communications RF/analog/mixed signal blocks, etc. In this flow, the design IP is brought to the physical design (for example, GDSII) file format. This block is then pushed through the RET tools flow, and the resulting RET-modified design is modeled in a virtual mask-writer, with new distortions peculiar to the write tool and process of the target mask shop. The ‘virtual mask’ shapes are then transformed by a model of the stepper imaging, resist development, and pattern transfer processes to create ‘virtual silicon patterns.’ These can be inspected for physical yield integrity (lack of shorting hazards, lack of unacceptable necking, etc.). They can also, especially in the case of electrical parasitic-sensitive blocks, be checked for electrical function integrity. For example, the ‘RET tools and flow’ block in Figure 4 should add dummy features, or ‘tiles.’ The function checker will then simulate the electrical effects of these new features on circuit function.

If there are yield or function issues, the re-design path of Figure 4 is executed and fixes the block well before designers begin integrating it into a full-chip design. This is a predictive engineering strategy of great power and deals in a fundamental way with the issues resulting from the fact that design is not equal to the silicon image. It fixes the consequent physical yield and circuit electrical parasitic failures at the design block level. It is critical that this flow not only be exercised to fix nominal problems, but also to correct for statistical ones relative to manufacturing tolerances. This latter point is very important. Sub-wavelength issues are significant at nominal exposure conditions, but even more significantly increase risk of failure as focus or exposure deviate from nominal in actual manufacturing. Consequently, statistical verification is a must.
When the true full chip integration and fabrication is implemented, as is described on the right side of Figure 4, the silicon image result is much more likely to be free of fundamental block-level issues. Remaining full-chip integration specific issues may be discovered at this stage, but they are as likely to be the classical ones that designers and tools address, namely architectural or full-chip timing and power verification issues rather than sub-wavelength distortion effects.

5.4 Post-RET

The complexities in mask data and manufacturing make it highly desirable to verify and optimize the mask data independently before committing to the costly fabrication process. An effective method for post-RET mask data verification is to simulate its image on the silicon wafer and compare it with the original design intent. This method places mask data in its intended operating environment and evaluate its performance metrics that have direct impact on wafer imaging. A simulation based verification system can evaluate the process for a product and give warning on certain performance limiting spots on the layout and thus significantly reduce the risk of mask data errors. Once the troubling spots are identified, localized corrections can be applied to extend the process window in an intelligent way.
The existing model based mask layout verification systems have a few areas that require further improvement. First, they are typically implemented with the same simulation engine with model based OPC. Sharing the simulation engine with OPC, the verification also inherits the errors of the OPC model. The logical dependency jeopardizes the probability of finding OPC errors, and reduces the reliability of the verification. A process window is the range of process parameter variations under which the line width remains within limits Secondly; they employ empirical modeling approaches that cannot easily track acceptable variations in process conditions. In order to sample a different condition in the process window, a different set of models has to be developed, which consumes significant effort and time.
In addition, there is no inherent reason why one set empirical models can judge the result of another if they are derived from the same set of mathematical formulation and training patterns. A full-featured photolithography simulator for mask data verification has been developed for the past decade by the major EDA vendors. (Mentor Graphics, Cadence) These types of simulators have been used extensively in lithography process development where they have demonstrated high accuracy for process predictions.
A mask data verification flow around the physical lithography simulation core that is independent from the OPC engine, thus free from the logical dependency between OPC and its verification. The use of physical models opens the possibility for achieving higher prediction accuracy on complex layout configurations. In addition, physical model can naturally predict the pattern transfer behavior under process variations such as focus change. Furthermore, a physical layout design can efficiently

leverage this physical model simulator to improve circuit performance and reduce the manufacturing variations.

6 Silicon Simulation

Silicon simulation is the capability to predict the pattern printed on silicon for a given layout. This is a complex task, as there are many factors in IC manufacturing that influence a silicon image, including original layout, mask process, stepper optics, photoresist characteristics, and develop and etch steps. Silicon simulation takes into account the impact of all these steps and characteristics on layout, and produces a simulated printed pattern that predicts what the layout would look like in silicon, without having to go through the costly and time-consuming manufacturing process. One of the applications using silicon simulation is silicon vs. layout verification, which uses simulation to compare the silicon "image" against the ideal "drawn" layout. Due to the nature of sub-wavelength issues, the last step in every sub-wavelength design must be silicon vs. layout verification.

Today, there are several valid "insertion points" for applying OPC. Most designers apply OPC at the end of the design cycle, once the design is entirely completed. This allows the OPC process for each geometry to take the proximity effects from all neighboring geometries into account and correct accordingly. Nevertheless, there are other design practices where OPC is embedded in the SoC IP (such as standard-cell libraries) or in the bit cells of embedded memories in order to ensure high manufacturing yield or performance tuning. It is also very conceivable that OPC may be done at different points during the design flow, depending on the nature of the block.

Sub-wavelength design methodologies and tools provide OPC capability in many different points during design flow, including at library creation; at custom-block creation; during integration of blocks; at physical verification; and during mask data preparation. Also, these tools support different styles of OPC as automatic vs. manual, rules-based, model-based and hybrid, and simple vs. aggressive corrections. These tools are flexible for integration of portions with different types and levels of OPC. Only through this flexible design methodology can the optimal level of OPC be applied to meet the performance, manufacturing-yield and mask manufacturing requirements of the design.

Phase aware physical design requires a physical-design environment (consisting of methodology and tools) that handles phase conflicts on a global and local scale, on the fly and in a transparent manner. The goal of phase aware design is to produce layouts that do not have any phase conflicts, and therefore guarantee success in manufacturing the corresponding mask set.

To that end, a phase aware physical-design tool must first detect possible phase conflicts that exist in the layout and transparently resolve them. By the same token, if an operation in any of these phase aware tools were to cause a phase conflict anywhere in the layout, the conflict would automatically be identified and avoided. Furthermore, since physical design tools also take timing into consideration (such as timing-driven placement), phase aware physical design tools must also take into account the effects of phase shifting on timing whenever applicable.

Major EDA vendors offer advanced tools for OPC and PSM. These are a ‘must have’ factors for manufacturing. Yet, as we are getting into 65 nm and below these methodologies need to be significantly modified in order to keep accurate manufacturing.

7 Lithography's Impact on Physical Design

Optical lithography is being pushed to new extremes especially with the move to 45 & 32nm processes. The extension of optical lithography has been enabled by several developments such as chemically amplified photoresists and anti-reflective coatings. By predicting physical phenomena (especially diffraction and interference) behind optical systems and systematically compensating for them, the minimum feature and pitch that can be resolved are significantly extended. This Resolution Enhancement Techniques (RETs) are aimed at three major optical wave components, namely, direction, amplitude and phase. Off Axis Illumination (OAI) techniques direct light at the photomask only at certain angles. The combination of the angle and the pitch of features in the mask can enhance resolution of certain pitches, particularly dense pitches and small lines. The design rules are complicated by the fact that certain large as well as certain fine pitches are well reproduced but some intermediate pitches may not print as well. This leads to some forbidden pitches and sizes.

Optical Proximity Correction (OPC) makes small alterations to the layout features to reduce line-width variation. Sub Resolution Assist Features (SRAFs) or scatter bars are added to the mask to allow isolated features diffract light as dense features but they do not print. Adding SRAFs to intermediate pitches can be tough resulting in suboptimal printing performance for these features. A concern here is that one might be perform double OPC action due to legacy design rules which lead to unnecessary constraints for designers as well as lithographers. The third category, phase, is controlled by Phase Shifting Masks (PSM). Parts of the mask are etched to create phase difference between regions and can enhance resolution for certain features by up to a factor of two. Generating phase-compliant layouts is a major problem for future physical design. An example consequence is the impact on routing algorithms. As we move into deep nanometer regime, some of the requirements such as spacing rules, reliability, signal integrity and process antenna rules impose severe constraints on routing algorithms. Some of these restrictive rules are listed below.

1. **Antennas** - Are formed by metal traces that accumulate static charge during manufacturing. Without a safe discharge path (through the reverse-biased diode at the output stage of a logic gate) any connected gate may be damaged due to electrostatic discharge. 'Antenna rules' establish maximum allowable ratios of metal area to gate area in the absence of discharge path. The pure router-based solution is bridging (layer-hopping) to limit the amount of metal connected to a gate; this creates more wiring, vias and congestion. The combined router and library-based solution is to drop reverse-biased diodes (source-drain contacts) close to the gate. Tightening of antenna ratios has lowered completion rates of detailed routers and led to more antenna waivers. Should liberal use of dioded cells be required, there will be high costs with respect to chip area and power metrics as well as non-trivial balancing of two sources of yield loss: increased die area versus antenna damage.

2. **Via stacking and minimum area rules** - Arise because stacking of vias through multiple layers can cause minimum area violations with respect to stacking dependent alignment tolerances. Signal routing layers are often divided into local layers, intermediate layers, and global layers. Layers within the same group have same pitches and parasitic. At the highest layer of a given group, the overhang of the 'up-via' can be significantly larger than that of the 'down-via. In addition, use of multiple-cut via cells to increase BEOL yield is complicated by dependencies on the layers and wire segment widths to be connected.

3. **Width- and length-dependent spacing rules** - Make minimum spacing a function of both wire width and length of parallel adjacencies. This means that edge costs during heuristic search are dependent on path history. Especially pernicious are influence rules (stub rules, halo rules), where a wide wire will influence the spacing rule within its surroundings. This results in strange jogs and spreading when wires enter an influenced area, as well as complicated ECO effects. Another aspect of reliability which is gaining prominence is resist pattern collapse. Resist features collapse upon formation at high aspect ratios. Pattern collapse probability is length dependent. This contributes to length-dependent spacing rules: longer parallel runs of wires require more spacing. Inserting jogs in the routing can avoid such effects.

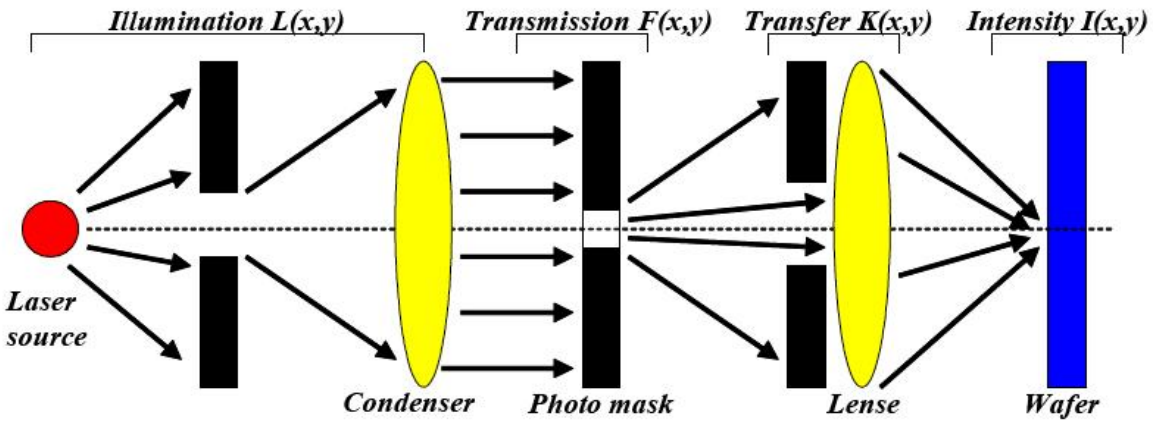


Figure #6 – Optical lithography system for VLSI manufacturing

8 Foundries Pre-Check Lithography

In order to handle uncertainties involved in design and manufacturing, new robust optimization techniques were explored. Emerging foundries these optimization techniques were embedded within Lithography process checks as part of custom hardware and software implementations of an additional verification step. After Tape-out layout scan, at the foundry and inside its mask operation, is already too late. Verification of a design for lithography and process compliance needs to happen within the layout editor, while constructing the layout, with an automatic and immediate feedback to the physical designer for compliance. This type of feature requires a model that considers the manufacturing process, and especially the lithography process, to the closest approximation. While foundries use their own OPC and RET models, sharing them with their customer base compromises their IP. Protection of this information is key element of the strategy for early RET implementation in the design flow. The solution is to encrypt the information, and then selectively allow customers to read certain levels of the information. In this

way, foundries can enable their customers to preview their designs, thereby greatly reducing turnaround time, as well as reduce the failure or reject rate at their end.

9 Smart Physical Design Tools

EDA physical design tools need to be tied more closely to manufacturing. The implementation of manufacturing issues into design rules and ultimately tech files, which will be read into layout and design tools, is creating new and intelligent generation of physical design tools. By embedding lithography awareness into the design space, adding RET tools to the custom IC and digital IC layout and routing tools and flows, designers are being given interactive checking capabilities that allow them to verify RET compliance during the design phase. Instead of the traditional 'DRV & LVS clean' Tape-out, we are getting lithography and process awareness built in functionality. The main idea is to embed several manufacturing subjects into physical design tools. For example, 'fracturing-aware design' may be a significant feature, whereby OPC, phase-shifter, and functional feature shapes are chosen or perturbed for reduced shot count. Layouts can also be stretched (via insertion of submicron-scale 'dead space') to help definition of major field boundaries (or, soft field boundaries) for mask writing. More complex extraction and characterization capabilities may also be required. Another aspect is physical design flow to consider manufacturing effects. Typically, design mask making and process engineering have depended on rule sets to isolate themselves from having to understand one another's technology. With number and complexity of these design rules exploding and ever decreasing yields, the traditional isolated deterministic design paradigm is breaking down. Close interaction between manufacturing, mask and design communities is inevitable. One of the most important aspects is to ensure predictable printability. New solutions being explored at the design end include regularity. Full chip layouts may need to be assembled as a collection of regular printable patterns for technologies beyond 65nm and 45nm has high likelihood for layouts to look like regular gratings: uniform pitch and width on metal as well as poly layers. Predictable layouts even in presence of focus and dose variations may be required. Several regular layout fabrics have been proposed with varying degrees of performance overhead and flexibility. FPGAs are very flexible but suffer from huge area, power and performance overheads. Via programmable gate arrays offer programmability of logic as well as interconnect using vias and contacts. These offer performance; power and area closer to ASICs as they do not have complex SRAM based programmable logic as FPGAs. Other examples of regular fabrics include Fishbone routing scheme and River PLAs. Somewhat less restrictive regularity can be achieved by more manufacturable cell libraries with regular structures which will require supportive placement techniques.

Before the final tape-out, it is verification time; the very last verification step is mask inspection. Die-to-database method is used to verify that the information on the mask is truly reflecting the design. With mask costs increase, finding defects at mask inspection turns out to be way too late. We now see many tools that inspect designs prior to tape-out, and verify the silicon intent in a simulated image against the original design.

Nevertheless, also this intermediate verification step is becoming too late. The solution is a preemptive check for manufacturing compliance during the physical design phase, cells or blocks, and scanning cell libraries for their adherence to lithography and manufacturing rules. True design-enabled lithography cannot be implemented as a post-design step, but rather needs to be embedded into the layout

tools and methodologies, so that designs can be concurrently checked and saved into libraries that are pre-verified for *both* mask manufacturing and silicon printing. New EDA concepts present lithography aware physical design which is fairly new concept function embedded into the mask flow. Hence mask writers work equally hard in perfecting a dummy fill shape, for example a company logo, a gate in a critical path, and a gate in a non-critical path; errors in any of these shapes will trigger rejection of the mask in the inspection tool. The result is overly low mask throughput and high mask costs. Another related objective of physical design can be to maximize the minimum CD tolerance over the whole layout. This can lead to better process window for lithographers as the process window is predominantly determined by the CD tolerance specification. Typically, a process is tuned to print a particular pitch very well. Moreover, this tuned pitch may be changed (for example by changing the nominal exposure) on a design-to-design basis. Physical design tools can then help choose the most critical pitch in the design which needs the most predictable and accurate printability.

10 Lithography-Clean-By-Construction concept has come of age

Even with newer RET methods, the traditional practice of applying these methods to the purely geometric data produced at final tape-out can offer only incremental improvements as design complexity increases. With the help of new EDA tools and flows, designers are starting to embed design information in manufacturing data, permitting downstream tools to optimize analysis on structures that are critical to the design.

At a more fundamental level, however, an emerging class of lithography-aware design tools allows designers to apply more proactive methods to ensure compliance with downstream lithographic requirements. Using sophisticated design rule sets that encode lithographic constraints, these tools allow designers to identify and correct problematic structures well before tape-out.

Using conventional tools, designers typically wait for manufacturing to determine if the design contained any structures that violate RET. Integrated in existing design flows, these litho-aware design tools allow designers to design for RET, OPC and PSM compliance. As designers create edges and place shapes, such tools provide immediate feedback to ensure that the layout will not violate subsequent OPC or phase shifting requirements. That's what we called Litho-Clean-By-Construction process. The system is based on a powerful new methodology that includes lithography analysis inside design flows. Embedded within design process, this powerful new method allows easy, transparent, and highly accurate litho-clean results. This new system, already included within design tools enables designers do not need to become lithography-experts, and neither do engineers on the fab floor have to have ultimate design intent knowledge. Since the technology is embedded within tools, its already automatically checks for manufacturing issues and mainly constraints, that can then be observed by the layout designer, thus creating 'lithography-clean-by-construction' on the fly. In a similar way, litho-aware methods can be implemented within placement and routing tools. The use-model is typically in an interactive way on a cell or block/macro level, with continued checks for RET compliance. In a litho-aware design tools cells will be interactively checked, and batched off into final libraries. In parallel all blocks or chip level run in a batch process to run final signoff verification. With this type of approach, designers can proceed to final tape-out, assured that the resulting manufacturing data is fully

lithography compliant. All fab's confidential IP which is embedded within the design flow needs to be protected. This can be easily done using well known encryption methods and limited, tiered access, based on the "need to know" basis information, targeted to the exact user level. (Figure #7)

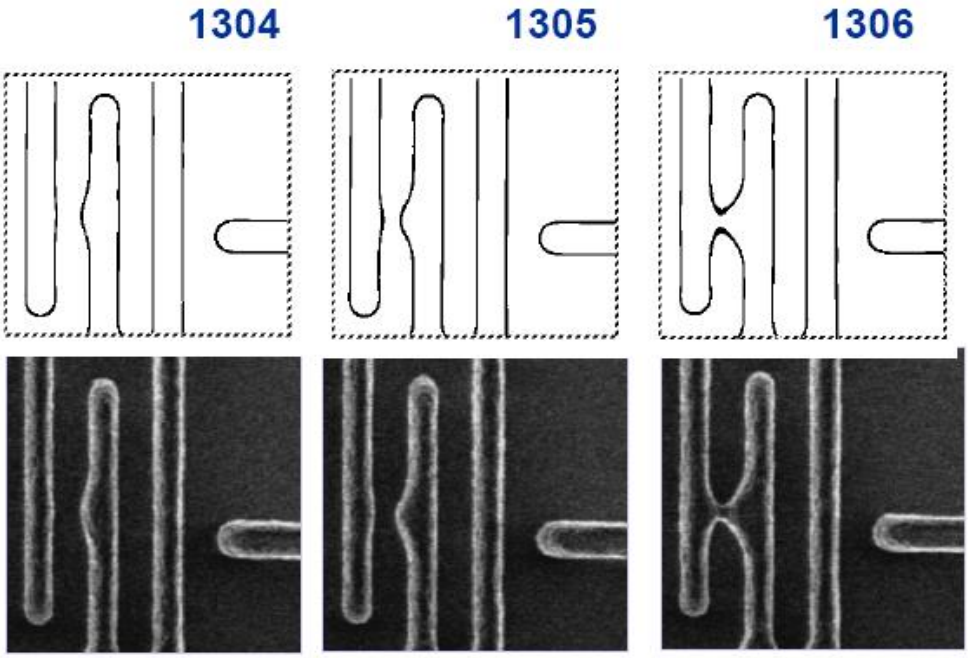


Figure #7 – Physical Design EDA tools 'Litho-Clean-By-Construction' approach

11 Conclusion

With the advancement of nanometer technologies IC designers are facing significant manufacturability challenges. Traditional methods for ensuring manufacturability like litho-simulations of IC designs are largely ineffective at advanced nanometer processes. In order to deal with sub-wavelength diffraction effects, emerging RET methods impose certain restrictions on the type of structures that can be reliably printed on silicon. In addition new concepts are implemented within design tools to ensure 'litho-correct-by-construction' designs. With the emergence of tools and methods that break down traditional boundaries between design and lithography, engineers can achieve optimal results in the shortest possible time. The continued evolution of design tools and flows that already include lithography-aware capabilities, offers increasingly effective strategies for ensuring manufacturability of more complex nanometer ICs. This new powerful approach used in upstream physical design tools provides a new generation of manufacturability-aware tools for advanced nanometer processes. The foundries are also joining the fight against 'nanometer effects' by providing lithography pre-checks, that are embedded (and encrypted for confidentiality) within design tools, to ensure manufacturability compliance at the design phase. While most current DFM solutions rely on either

rule-based optimization or post-layout enhancement guided by modeling, there are tremendous ongoing research and development to capture the downstream manufacturing and process effects, to abstract them early on into the key physical design stage, through model-based manufacturability aware routing optimization. This allows designers to perform more global optimization for manufacturability and yield in the context of other design objectives such as timing, power, area, and reliability. As manufacturability aware technologies are constantly under heavy research, there are many topics to improve in terms of process modeling or abstraction and DFM-routing or connectivity algorithms, to enable true design for manufacturing. Most current optimizations for DFM are performed independently, but different DFM issues are indeed highly related with each other such as critical area, lithography, CMP, and redundant via. The improvement of one aspect may make other aspects worse, and vice verse. This is causing a complicate challenge for the EDA industry that is trying to support the semiconductor industry for the actual DFM issues. No Doubt, it is a constant race after the advancement of nanometer technologies.

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